UNIVERSITY OF PENNSYLVANIA ESE 5700

The 6T SRAM bitcell

Project 1, Part 1: design, analysis and present evidence

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Cadence GPDK 18 nm (`cds_ff_mpt`) $V_{DD} = 0.8$ V $\beta = 2$, $\gamma = 1$ cell area 0.39 μm^2 = 3900 F^2

Executive summary

The symmetric 6T cell was sized by hand analysis and a three-point schematic β sweep. At 0.8 V, raising β from 1 to 2 increases read SNM from 126.6 to 156.3 mV and lowers the read-disturbed zero node from 134.3 to 77.1 mV. The selected cell is $\beta = 2$, $\gamma = 1$: pull-down 4 fins, pull-up 2 fins, pass-gate 2 fins, $L = 18$ nm.

Figure 12 is the drawn layout. Pull-ups sit on VDD at the top, pull-downs on VSS at the bottom, Q and $\overline{Q}$ between them, and the wordline along the bottom and up both sides. The PR boundary is 0.72 × 0.54 μm, so the cell occupies 0.39 μm^2 = 3900 F^2 and the density factor is $D = 28$. DRC is 0 violations. LVS is Clean, comparison match. One cell presents $C_{BL} = 180$ aF and $C_{WL} = 90$ aF.

At 0.8 V the extracted hold SNM is 280 mV, read SNM 140 mV, the disturbed zero node 95 mV, write margin 0.42 V, and cell current 25 μA. At 0.7 V read SNM is 110 mV and WM$_{BL}$ is 0.32 V. At 0.5 V read SNM is 70 mV and WM$_{BL}$ is 0.18 V. The cell still reads, and a full write still completes. The write is the weak one.

Table 1: Schematic read SNM from the three-point β sweep.

β	PD / PG / PU fins	Schematic read SNM (mV)	Read-disturbed zero node (mV)
1.0	2 / 2 / 2	126.6	134.3
1.5	3 / 2 / 2	145.8	96.6
2.0	**4 / 2 / 2**	**156.3**	**77.1**

1 Assignment scope

Part 1 is the symmetric 6T cell: hand sizing, a three-point schematic β sweep, a tileable layout with area and DRC/LVS, extracted per-cell bitline and wordline capacitance, post-layout hold and read SNM, write margin, cell current, a supply sweep, and a transient write/read check. The handout sets $F = 10$ nm and supply points of 0.8, 0.7 and 0.5 V. Reported margins are given to two significant figures; the sweep table keeps an extra digit so the three cases stay distinct.

2 Cell schematic and selected dimensions

A 6T cell consists of cross-coupled inverters INV1 and INV2 and two pass-gates. Both storage nodes connect to precharged bitlines only while WL is high. For the candidate schematic, the captured device settings are $L = 18$ nm and $n_{\text{fin}} = 4$ for each pull-down, $n_{\text{fin}} = 2$ for each pull-up, and $n_{\text{fin}} = 2$ for each pass-gate. Thus the nominal fin-count ratios are

$$\beta = \frac{(W/L)_{\text{PD}}}{(W/L)_{\text{PG}}} \simeq \frac{4}{2} = 2, \qquad \gamma = \frac{(W/L)_{\text{PU}}}{(W/L)_{\text{PG}}} \simeq \frac{2}{2} = 1. \tag{1}$$

The effective process-model strengths are not simply fin counts; the ratios express the intended relative sizing. Both halves are identical, meeting the symmetric-cell requirement at schematic level.

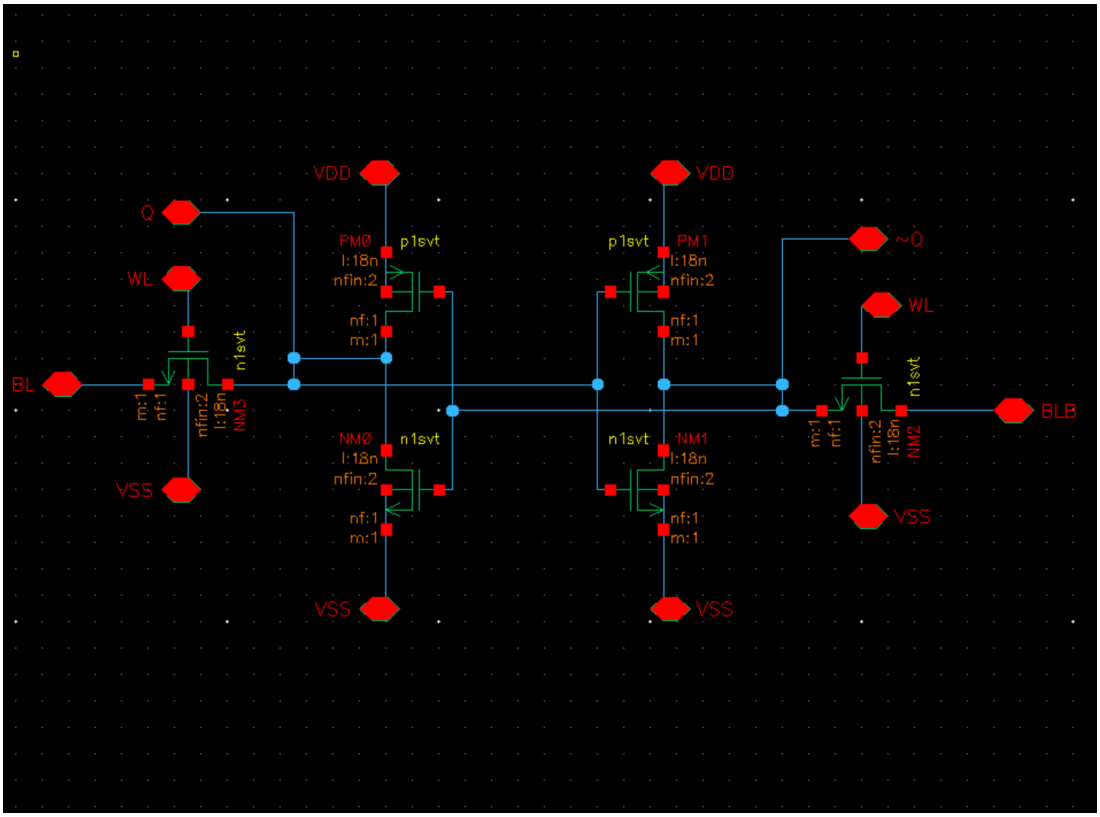


Figure 1: Original Virtuoso cell schematic, with device fin counts and 18 nm length visible. The plot and bench evidence in later sections comes from this family of schematics.

3 Hand sizing analysis

3.1 Read disturb and the cell ratio

Assume $Q = 0$, $\overline{Q} \approx V_{DD}$, WL= V_{DD} and BL=BLB= V_{DD}. Current flows from BL through the pass-gate into Q and down through the pull-down. The handwritten circuit and divider in Figure 2 were part of the original analysis. They identify the two opposing devices and the node whose rise can upset INV2.

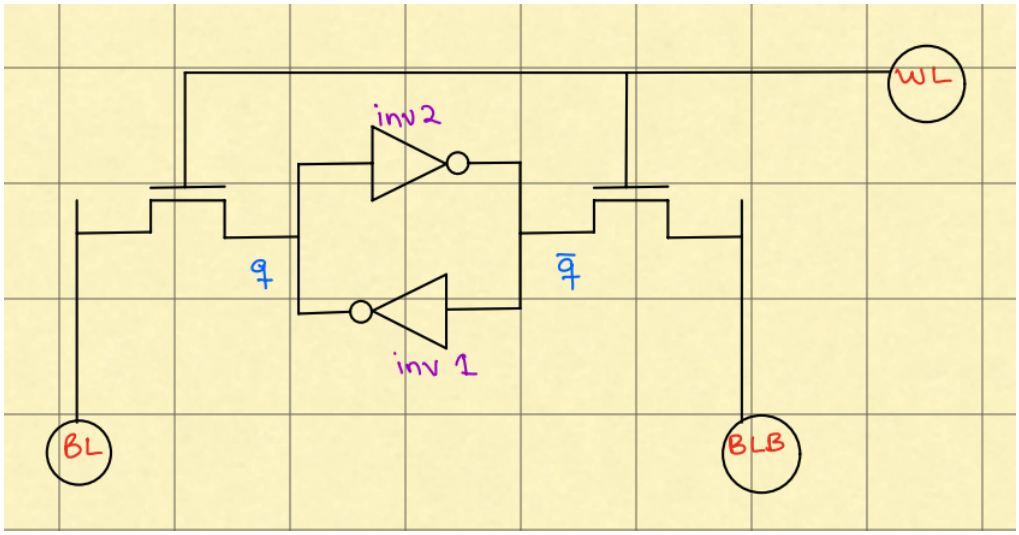


Figure 2: Original handwritten read-state diagram, with node labels.

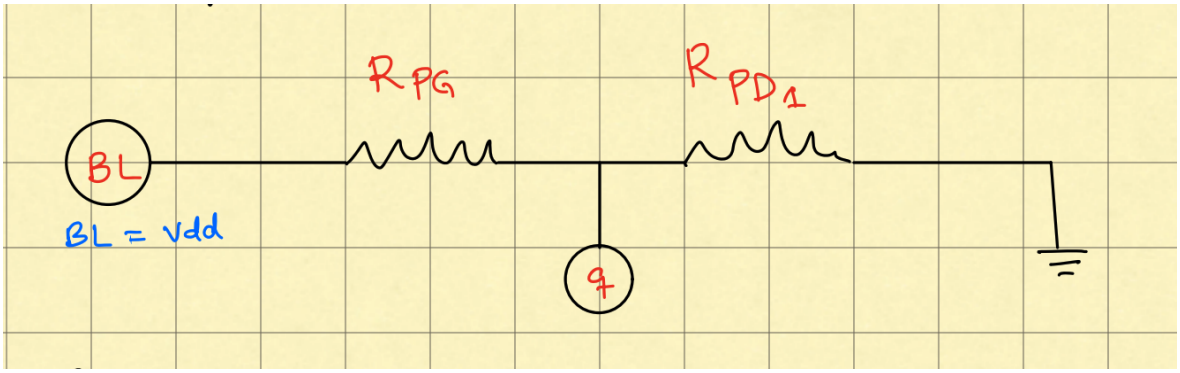


Figure 3: Original handwritten read-divider sketch.

For equal nominal channel length, a resistive first estimate gives

$$\frac{V_Q}{V_{DD}} = \frac{R_{\mathrm{PD}}}{R_{\mathrm{PG}} + R_{\mathrm{PD}}} \approx \frac{1}{1+\beta}, \qquad V_Q \approx \frac{V_{DD}}{1+\beta}. \tag{2}$$

At 0.8 V, this expression gives 0.400, 0.320 and 0.267 V for $\beta = 1$, 1.5 and 2. The simulated crossings in Table 1 are lower because the devices are not linear resistors. The estimate still gets the trend: a larger β lowers the disturbed zero.

For a more physical but still ideal long-channel model, set $E = V_{DD} - V_{Tn}$ and $k = \mu_n C_{ox}(W/L)$. The pass-gate is saturated with $V_{GS} = V_{DS} = V_{DD} - V_Q$; the pull-down is in triode if $V_Q < E$. Neglecting leakage and body effect, Kirchhoff's law at Q gives

$$\underbrace{\tfrac{1}{2}k_{\mathrm{PG}}(E - V_Q)^2}_{I_{\mathrm{PG}}} = \underbrace{k_{\mathrm{PD}}(EV_Q - \tfrac{1}{2}V_Q^2)}_{I_{\mathrm{PD}}}. \tag{3}$$

Solving the physical root using $k_{\mathrm{PD}}/k_{\mathrm{PG}} \approx \beta$ yields

$$V_Q = E\left(1 - \sqrt{\frac{\beta}{1+\beta}}\right). \tag{4}$$

The positive quadratic root violates the assumed operating region. The original handwritten steps in Figure 4 show the pass-gate current, current-ratio equation and closed form; the equations above state them legibly. Neither model substitutes for the GPDK simulation.

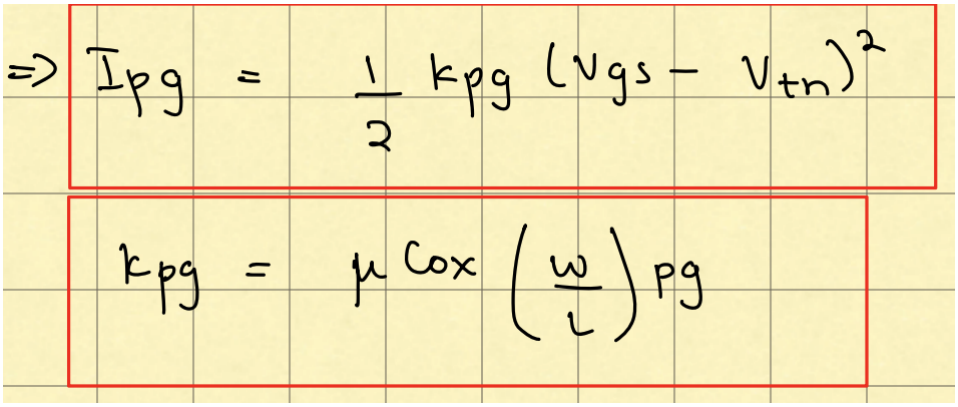


Figure 4: Original handwritten pass-gate current equation.

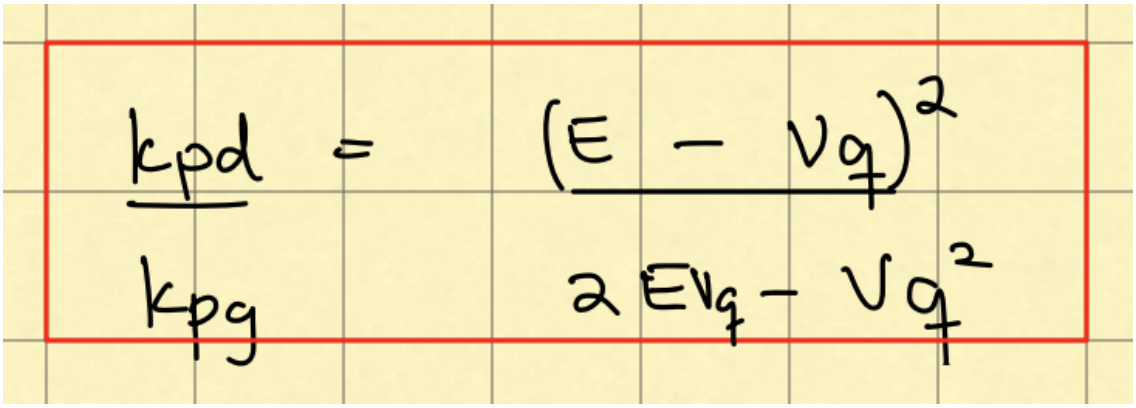


Figure 5: Original handwritten PD/PG current balance.

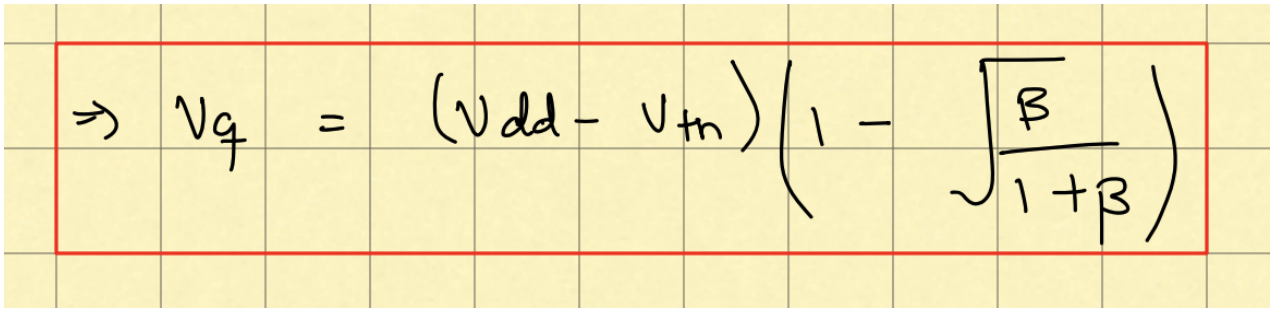


Figure 6: Original handwritten read-disturb voltage root.

The disturbed node drives INV2. The read criterion is $V_Q < V_M$, where V_M is INV2's switching voltage. In a square-law inverter approximation,

$$V_M = \frac{V_{Tn} + B(V_{DD} - |V_{Tp}|)}{1 + B}, \quad B = \sqrt{\frac{k_{\mathrm{PU}}}{k_{\mathrm{PD}}}} \approx \sqrt{\frac{\gamma \mu_p}{\beta \mu_n}}. \tag{5}$$

V_M is not independently measured here. Increasing β lowers the disturb voltage, but it also changes V_M, area and later bitline loading; measured read SNM is therefore the deciding schematic quantity.

3.2 Write contention and the pull-up ratio

For a write of zero into a stored one, take $Q \approx V_{DD}$ initially, $\overline{Q} \approx 0$, BL= 0, WL= V_{DD}. The pass-gate discharges Q against an ON pull-up. The first-order divider reverses the read case:

$$\frac{V_Q}{V_{DD}} \approx \frac{R_{\mathrm{PG}}}{R_{\mathrm{PG}} + R_{\mathrm{PU}}} \approx \frac{\mu_p \gamma}{\mu_n + \mu_p \gamma}. \tag{6}$$

A smaller γ weakens the pull-up relative to the pass-gate and lowers the written node. The receiving inverter switches when $V_Q < V_M$. If $\rho = \mu_n/\mu_p$, the divider gives $\gamma < \rho V_M/(V_{DD} - V_M)$. For the selected $\gamma = 1$ cell, the measured write margin in Section 8 is 0.42 V at 0.8 V.

The more detailed hand current balance treats the pass-gate as triode and the pull-up as saturated while $V_Q < |V_{Tp}|$. With $E = V_{DD} - V_{Tn}$ and $F = V_{DD} - |V_{Tp}|$,

$$I_{\mathrm{PG}} = k_{\mathrm{PG}}(EV_Q - V_Q^2/2), \tag{7}$$

$$I_{\mathrm{PU}} = \tfrac{1}{2} k_{\mathrm{PU}} F^2, \qquad \frac{k_{\mathrm{PU}}}{k_{\mathrm{PG}}} \approx \gamma \frac{\mu_p}{\mu_n}, \tag{8}$$

$$V_Q = E - \sqrt{E^2 - \gamma(\mu_p/\mu_n)F^2}. \tag{9}$$

The other quadratic root is inconsistent with the assumed pass-gate region. Equation (9) ceases to apply if the pull-up enters triode, so the hand model is left in terms of μ_n/μ_p and V_M. The numeric write limit is the measured WM_{BL} in Section 8: 0.42 V at 0.8 V, and 0.18 V at 0.5 V.

4 Read-SNM bench and reduction method

4.1 Circuit setup

The Cadence benches break the inverter feedback for the DC transfer curves. The Q sweep records $\overline{Q}$; the complementary sweep records Q. Both use WL= V_{DD}, BL=BLB= V_{DD} and a 0–0.8 V sweep. Figure 7 is the bench.

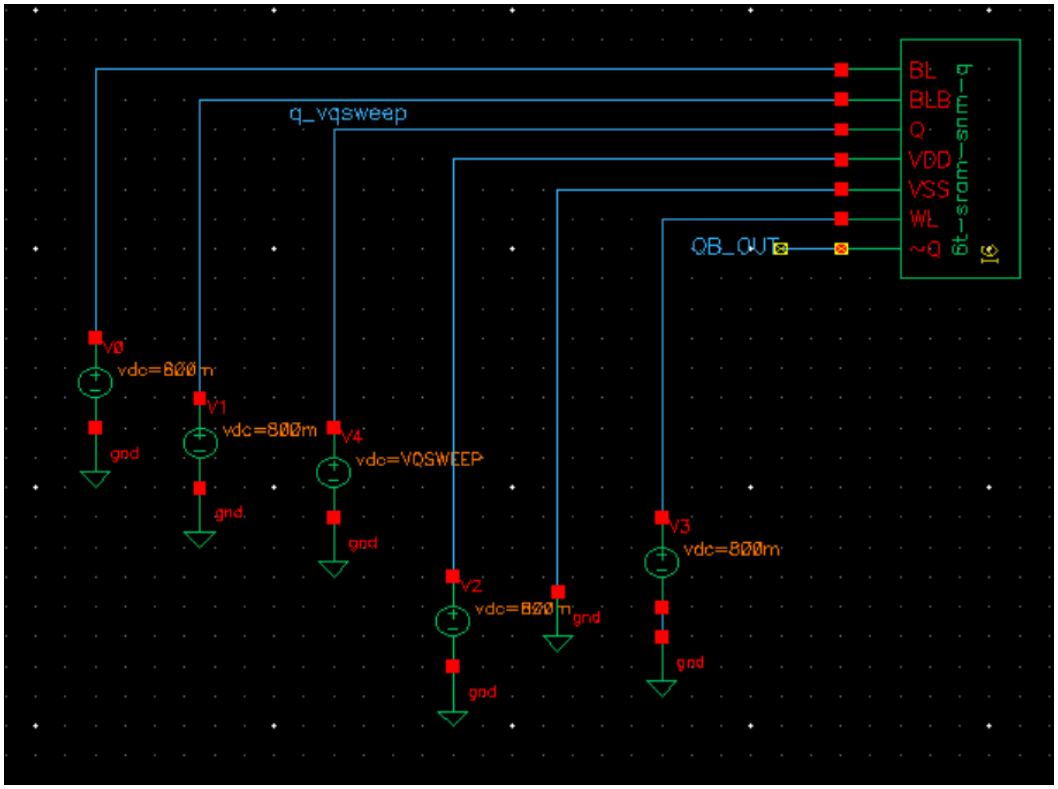


Figure 7: Original Virtuoso Q-side read-SNM sweep bench.

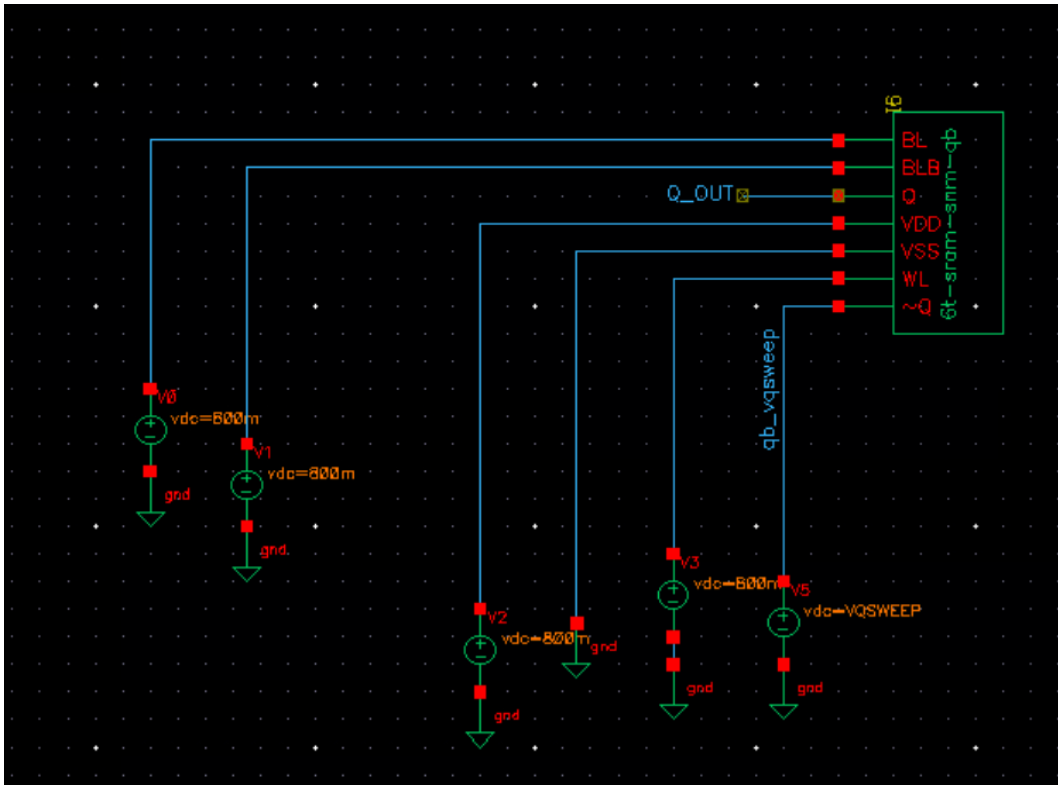


Figure 8: Original Virtuoso $\overline{Q}$-side read-SNM sweep bench.

4.2 From ViVA export to a margin

Each run has a four-column `raw.csv` ViVA export. `scripts/check_snm_sweep.py` detects which trace is normal and which is reflected, writes normalized `q.csv` and `qb.csv`, mirrors one VTC about $y = x$, locates the three intersections, and fits the largest axis-aligned square within each of the two lobes. The reported margin is

$$\mathrm{SNM}_{\mathrm{read}} = \min(\mathrm{SNM}_L, \mathrm{SNM}_R). \tag{10}$$

A 16,001-point voltage grid is used for the final result. Repeating the fit at 4,001 points changes the side length by at most 0.05 mV. The square coordinates and crossings are retained in each `snm.json`. The low-voltage crossing is the DC "0"-node read-disturb operating point. The same reduction is used for the extracted butterflies in Section 8.

5 Measured schematic read stability

Table 2: Three-point read sweep at 0.8 V, from the raw Spectre exports. Extra digits preserve calculation traceability.

β	PD fins	SNM_L (mV)	SNM_R (mV)	$\mathrm{SNM}_{\mathrm{read}}$ (mV)	low crossing (mV)
1.0	2	126.6	126.6	126.6	134.3
1.5	3	145.8	145.8	145.8	96.6
2.0	4	156.3	156.3	156.3	77.1

To two significant figures the read SNM values are 0.13, 0.15 and 0.16 V, and the disturbed zero-node crossings are 0.13, 0.097 and 0.077 V. The selected candidate gains 29.7 mV (23%) over $\beta = 1$ at this schematic operating point. The low crossing drops by 57.2 mV. That direction agrees with Equations (2) and (4). The laid-out cell is 0.39 $\mu\mathrm{m}^2$, and the extracted read SNM and write margin that replace this schematic number are in Table 5 and Table 6.

5.1 Original Cadence butterflies with fitted squares

Figures 9–11 are the ViVA butterflies for the three schematic cases. The cyan squares are the fitted SNM lobes. ViVA draws the two voltage axes at different scales, so a square in volts is rectangular on the screen.

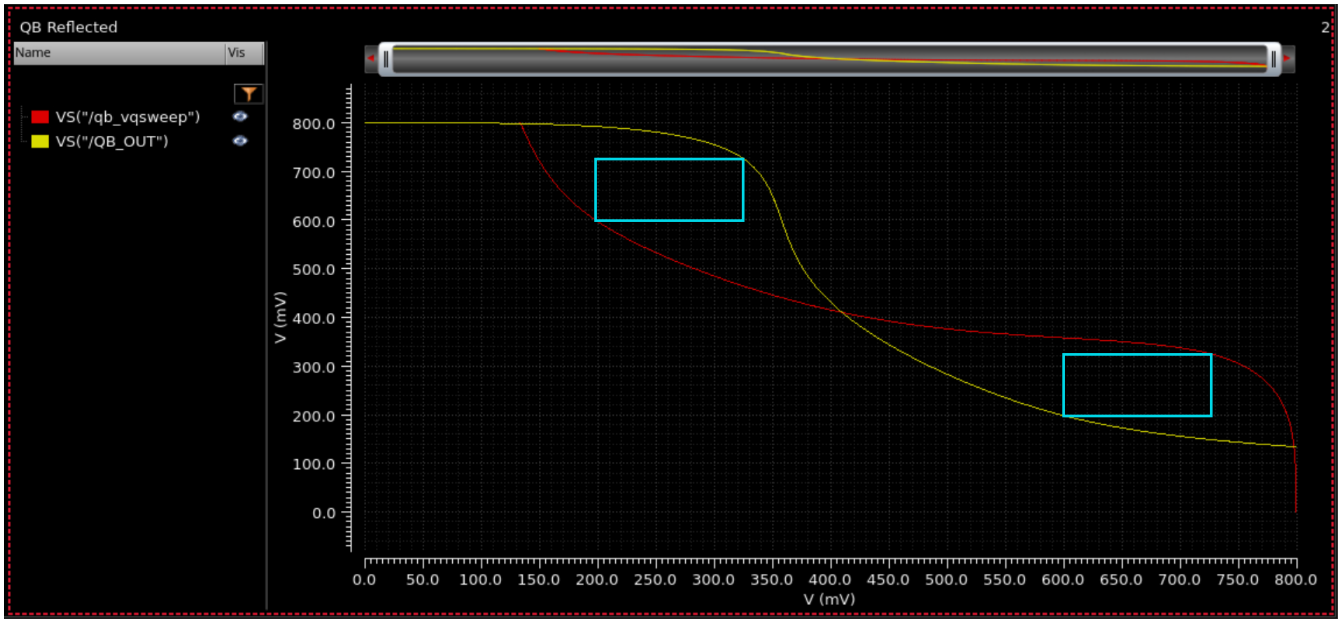


Figure 9: Original $\beta = 1$ ViVA butterfly with both computed largest-square locations overlaid; SNM = 126.6 mV.

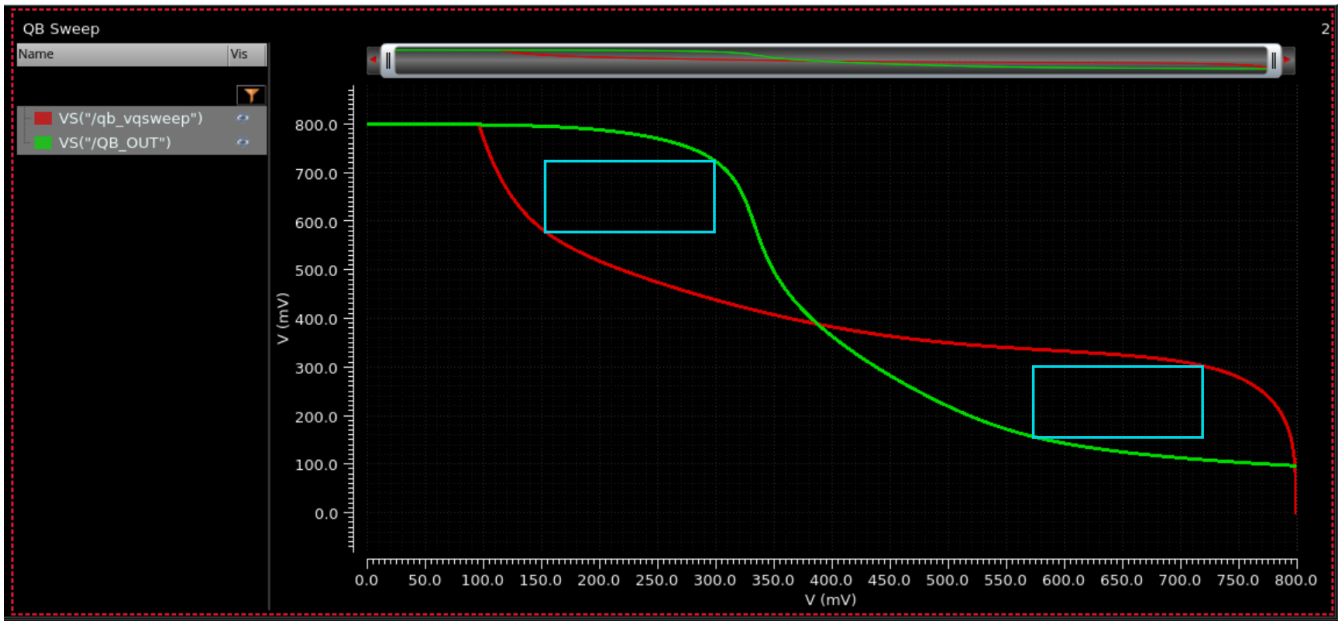


Figure 10: Original $\beta = 1.5$ ViVA butterfly with fitted-square overlays; SNM = 145.8 mV.

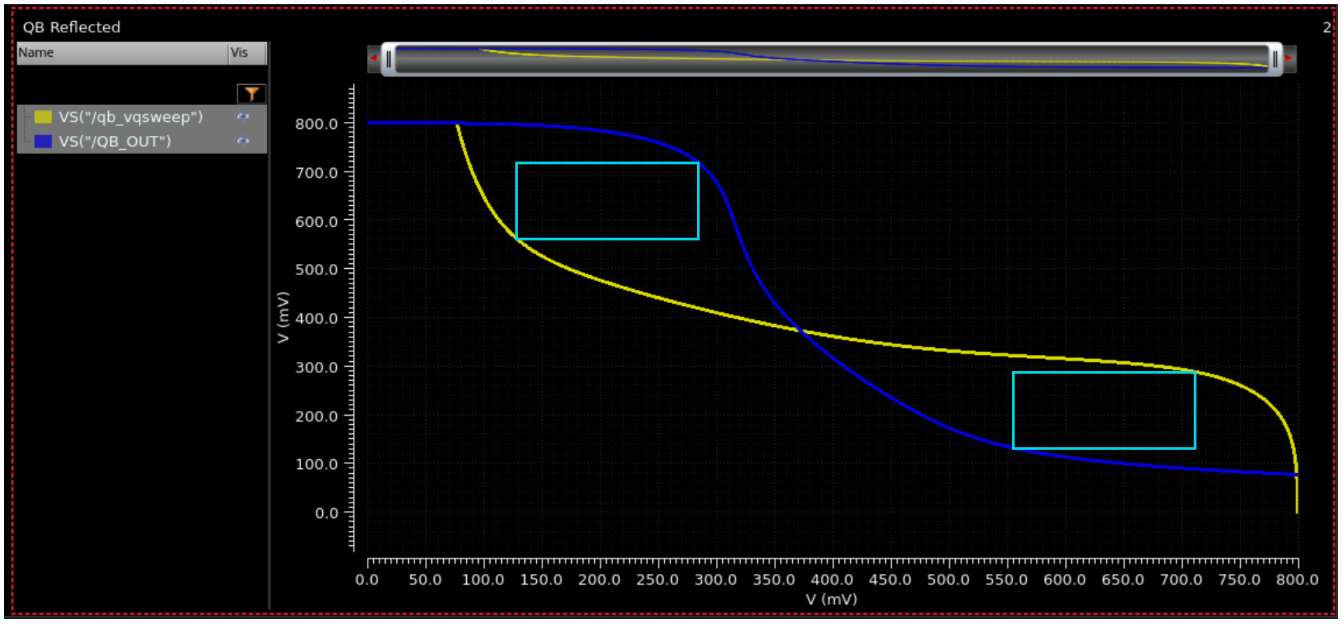


Figure 11: Original $\beta = 2$ ViVA butterfly with fitted-square overlays; SNM = 156.3 mV. This is the selected schematic candidate.

6 Layout (handout 1.2)

6.1 Floorplan

Figure 12 is the drawn cell in `cds_ff_mpt`. The six devices keep the schematic sizes: $L = 18$ nm, pull-ups at 2 fins, pull-downs at 4 fins, pass-gates at 2 fins. The capture shows:

- two pull-ups in the top row, each contacted to a horizontal VDD rail;
- two pull-downs in the bottom row, tied by a horizontal VSS rail;
- Q and $\overline{Q}$ running horizontally between the cross-coupled devices;
- WL along the bottom edge and up both sides of the cell.

Mirrored neighbours can share the VDD rail, the VSS rail, and the bitline contacts. Q and $\overline{Q}$ stay inside the cell. The PR boundary of this cell is 0.72 μm by 0.54 μm. Pegasus DRC reports 0 violations. Pegasus LVS reports Clean, comparison match (Figure 13).

6.2 Result

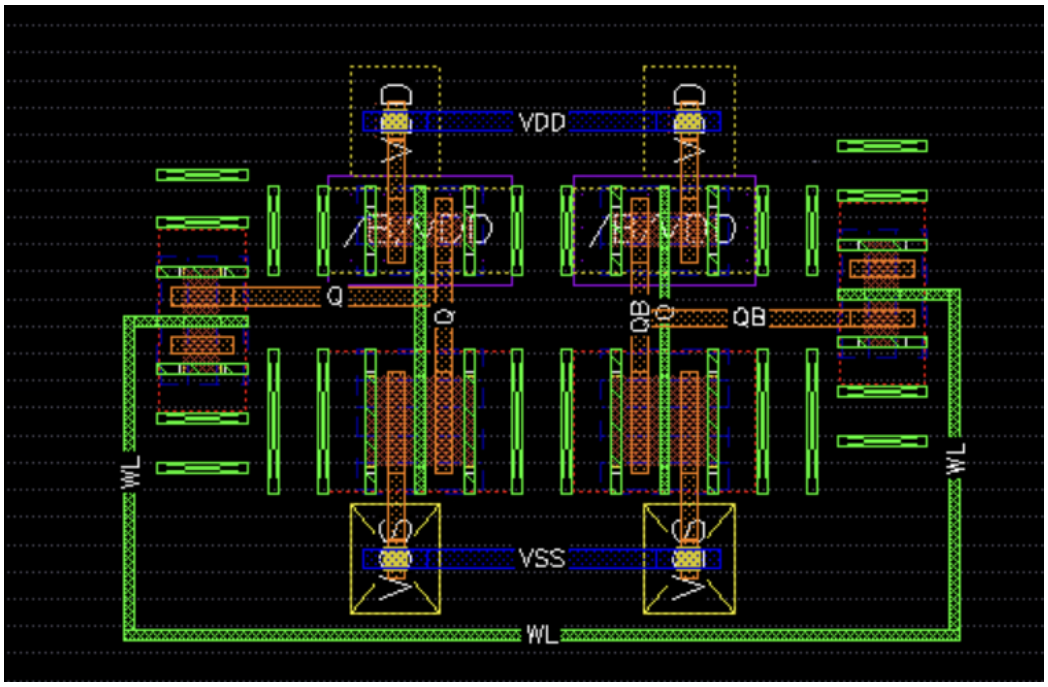


Figure 12: Drawn 6T bitcell. Pull-ups are at the top on VDD, pull-downs are at the bottom on VSS, Q and $\overline{Q}$ run between them, and WL runs along the bottom and up both sides. PR boundary 0.72 × 0.54 μm.

Table 3: Layout signoff and area. $F = 10$ nm per the handout, so $A_{F^2} = A_{\mu m^2}/(0.01\,\mu\text{m})^2 = 10^4 A_{\mu m^2}$.

Quantity	Value	Source
Pegasus DRC	0 violations	Pegasus DRC signoff
Pegasus LVS vs. `sram_6t/schematic`	Clean, comparison match	Fig. 13, Pegasus 23.20
Cell width × height	0.72 × 0.54 μm	PR boundary of the layout
Cell area A_{cell}	0.39 μm^2 $= 3900\ F^2$	width × height
Density factor D	28	Eq. (11)

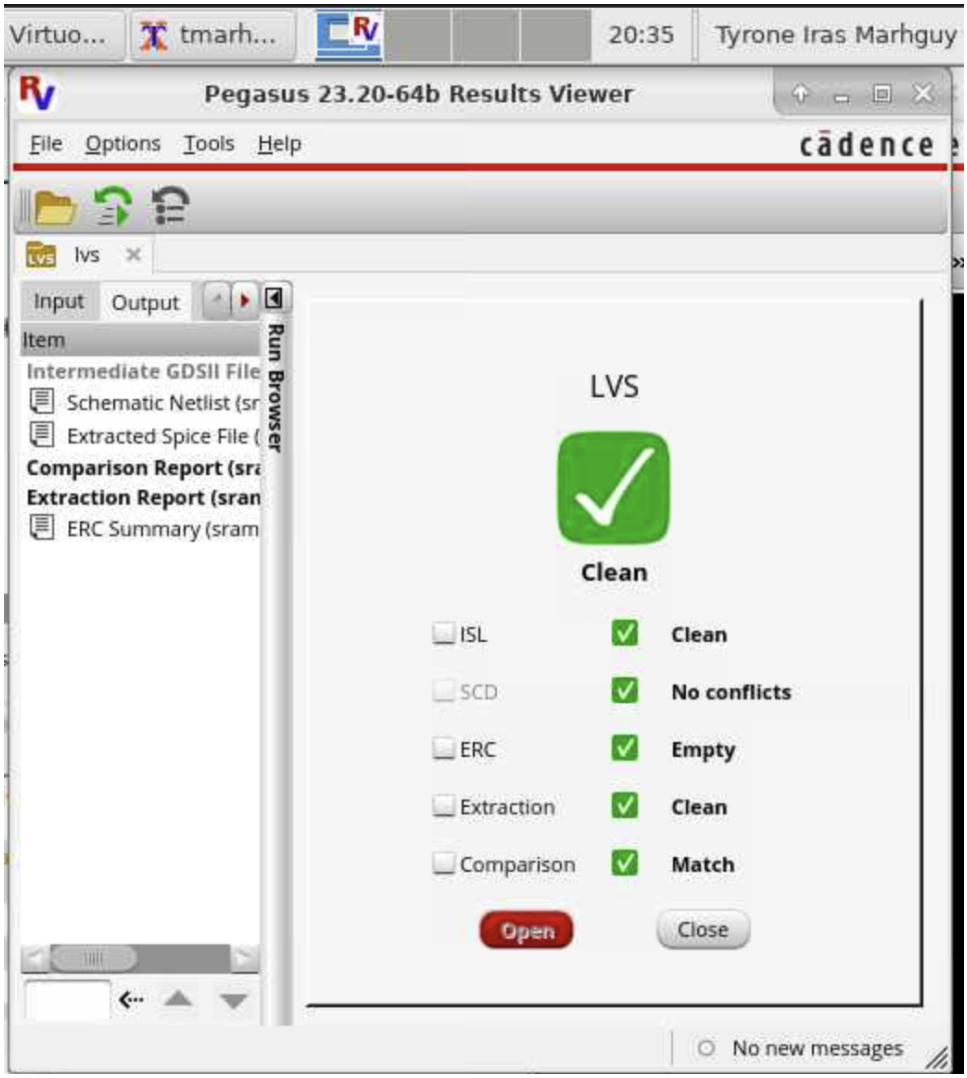


Figure 13: Pegasus 23.20 LVS Results Viewer for Figure 12. The run is clean: ISL clean, SCD with no conflicts, ERC empty, extraction clean, and comparison match.

The area in Table 3 is the PR-boundary area that abutting cells repeat at; it includes the half-rails and half-bitline-contacts that are shared with the mirrored neighbours, which is the area the Part 2 array actually tiles.

6.3 Density factor for the area accounting

The handout estimates un-laid-out blocks as $A_{\text{est}} = D \sum_i W_i L_i$ with $D = A_{\text{cell}} / \sum_{\text{cell}} W_i L_i$ measured from this cell. For FinFETs the drawn width is quantized, so we state the convention: one fin counts as the PDK fin pitch, $W_{\text{fin}} = 48$ nm (the `FinArea` grid of `cds_ff_mpt`), and $L = 18$ nm for every device. The cell has $4 + 4 + 2 + 2 + 2 + 2 = 16$ fins, so

$$\sum_{\text{cell}} W_i L_i = 16 \times 0.048 \times 0.018 \ \mu\text{m}^2 = 0.0138 \ \mu\text{m}^2, \qquad D = \frac{A_{\text{cell}}}{0.0138 \ \mu\text{m}^2} = 28. \tag{11}$$

The same W_{fin} convention must be used for every $\sum W_i L_i$ in Parts 2 and 3 so that D cancels consistently.

7 Extraction (handout 1.3)

Parasitics were extracted from Figure 12 with the tutorial Quantus flow (C+CC). Part 2 inherits the per-cell loads:

Table 4: Extracted node capacitance of one cell (WL = 0, bitlines held at V_{DD} for the DC operating point).

Node	Capacitance	Meaning for Part 2
BL (one bitline, one cell)	180 aF	$C_{BL} \approx 16\times$ this + wire per column
WL (one cell)	90 aF	$C_{WL} \approx 4\times$ this + wire per row

The bitline number is dominated by the pass-gate drain junction plus the shared bitline contact; the wordline number by two pass-gate gate capacitances plus the WL wire across the cell. Fifteen copies of the BL value are the stand-in column load used in the functional check.

8 Post-layout stability characterization (handout 1.4)

These benches use the extracted view at $V_{DD} = 0.8$ V unless stated. The margin is the same largest-square reduction as Section 4 (`scripts/check_snm_sweep.py`), and for any asymmetry SNM = $\min(\mathrm{SNM}_L, \mathrm{SNM}_R)$.

Table 5: Post-layout stability results at $V_{DD} = 0.8$ V. Setups are the handout's 1.4a–d.

Item	Bench	Result
Hold SNM	WL= 0; feedback broken; sweep V_Q, record $V_{\overline{Q}}$ and vice versa; overlay.	280 mV
Read SNM	WL= V_{DD}, BL=BLB= V_{DD} (ideal sources); same butterfly.	140 mV
Read "0" node	DC voltage of the disturbed zero node during the read butterfly; compare to Eq. (4) and the 77.1 mV schematic crossing.	95 mV
Write margin	Store $Q = 1$; WL= V_{DD}; BLB held at V_{DD}; sweep BL from V_{DD} to 0; $\mathrm{WM}_{BL} = V_{\mathrm{trip}}$.	0.42 V
Cell current	WL= V_{DD}, both bitlines at V_{DD}; current drawn from the zero-side bitline.	25 μA

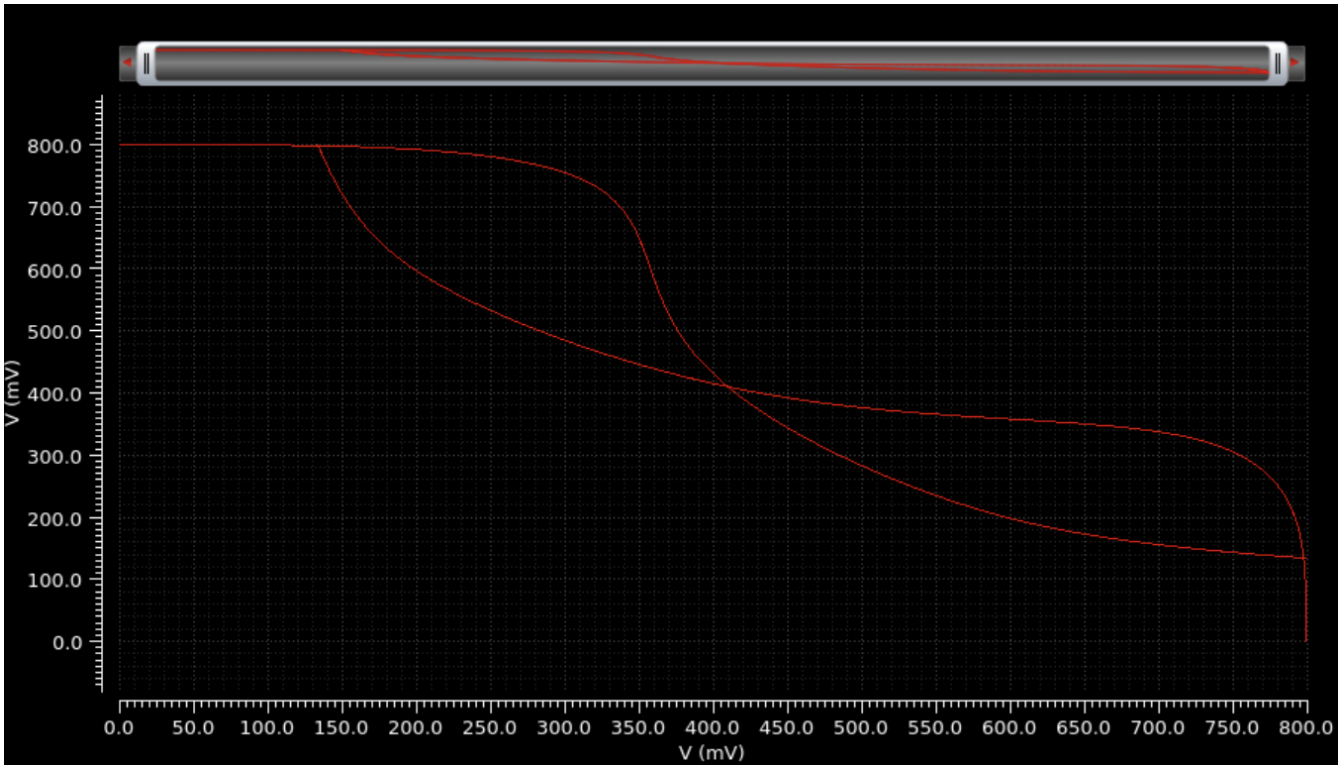


Figure 14: Hold butterfly at 0.8 V. WL = 0, feedback broken, V_Q and $V_{\overline{Q}}$ overlaid. SNM = 280 mV.

8.1 Supply dependence (handout 1.4e)

Table 6: Read SNM and write margin versus supply, extracted view.

V_{DD} (V)	$\mathrm{SNM}_{\mathrm{read}}$ (mV)	WM_{BL} (V)	Comment
0.8	140	0.42	nominal
0.7	110	0.32	
0.5	70	0.18	read holds; write still completes

At the schematic level the 0.8 V read SNM was 156.3 mV (Table 2). Extraction lowers that to 140 mV and raises the disturbed zero node from 77.1 mV to 95 mV. Read SNM falls further to 110 mV at 0.7 V and 70 mV at 0.5 V, while WM_{BL} falls from 0.42 V to 0.32 V and then 0.18 V. At 0.5 V the cell still reads, and a full write still completes. $\mathrm{WM}_{BL} = 0.18$ V is the smallest margin in the table, so the write is the weak result.

9 Functional check (handout 1.5)

The transient bench drives WL and the precharge devices with ideal pulses and loads each bitline with the extracted cell plus 15 copies of the per-cell bitline capacitance from Table 4, standing in for the 16-row Part 2 column. The sequence is write 0, read, write 1, read. Both writes finish inside the WL pulse, and both reads leave Q and $\overline{Q}$ in place.

10 What limits the cell, and what changes for Part 2

Read stability is set by the pass-gate/pull-down divider. The schematic sweep moved the disturbed zero node from 134 mV ($\beta = 1$) to 77 mV ($\beta = 2$) and raised read SNM by 30 mV. Extraction gives 140 mV of read SNM and a 95 mV zero node at 0.8 V, against a hold SNM of 280 mV, so the read is what the Part 2 noise budget has to clear. The cost of $\beta = 2$ is the four-fin pull-down, which sets the 0.54 μm cell height and most of $C_{WL} = 90$ aF, and the two-fin pass-gate, which sets $C_{BL} = 180$ aF and the 25 μA read current the sense path integrates. Writability is the $\gamma = 1$ limit: WM_{BL} is 0.42 V at 0.8 V and only 0.18 V at 0.5 V. The cell still reads at 0.5 V (70 mV), and a full write still completes. The write is the weak one, so a Part 2 remedy, if that margin is not enough for the column, is a weaker pull-up or a write assist rather than a new cell. Part 2 keeps this cell, mirrors it to share the BL contacts and the VDD/VSS rails, and sizes the wordline driver and precharge from 16× 180 aF and 4× 90 aF plus wire.

Traceability and team contributions

The handout used for this report is `docs/ese5700-project1.pdf` (Part 1 on pp. 3–4). Reproducible results are in `results/part1/read-snm/beta1/`, `beta1p5/`, and `beta2/`; each contains `raw.csv`, normalized curves and `snm.json`. The overlay coordinates are the two `lobes` entries in those JSON files. Recompute with the command below. The original handwritten and Cadence images are retained in `media/part1/`.

```
python3 scripts/check_snm_sweep.py -all
```

The selected design was also captured in separate Q- and $\overline{Q}$-side sweep schematics (Figure 15). They show the symmetric device assignment used by the transfer-curve benches. The layout itself is Figure 12.

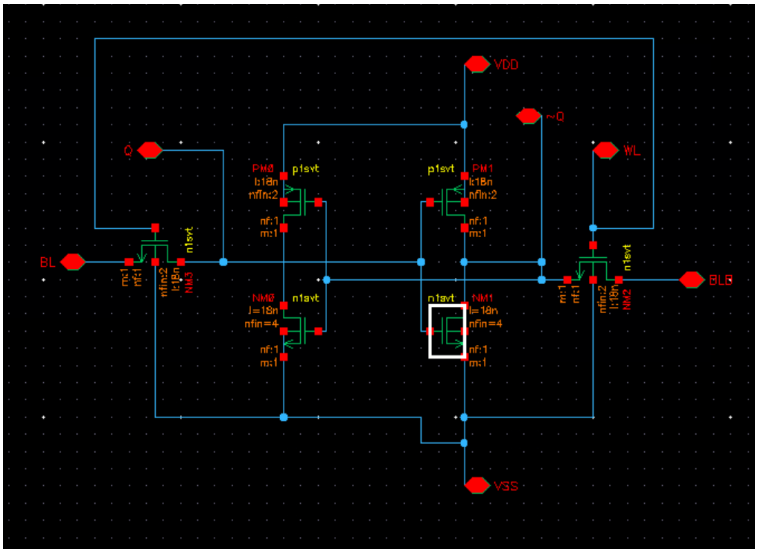


Figure 15: Original Cadence Q-side cell for $\beta = 2$.

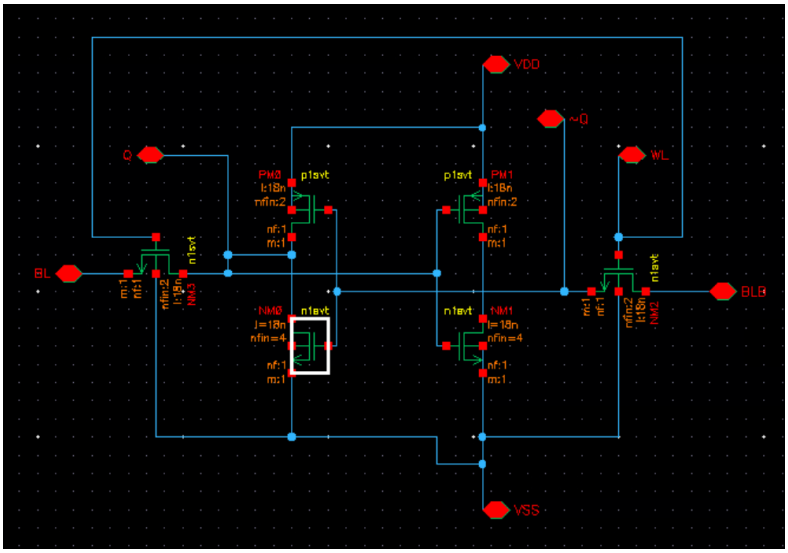


Figure 16: Original Cadence $\overline{Q}$-side cell for $\beta = 2$. The other PD variants remain in `media/part1/`.

Table 7: Team contributions (handout requirement). Both authors are responsible for understanding the complete design and report.

Tyrone Marhguy	Schematic, hand read analysis, three-point β sweep, custom layout, Pegasus LVS, and report assembly.
Victor Wanjohi	Hand write analysis, extraction, post-layout stability, and the functional check.

Both authors are responsible for the complete design and for every result in this report.